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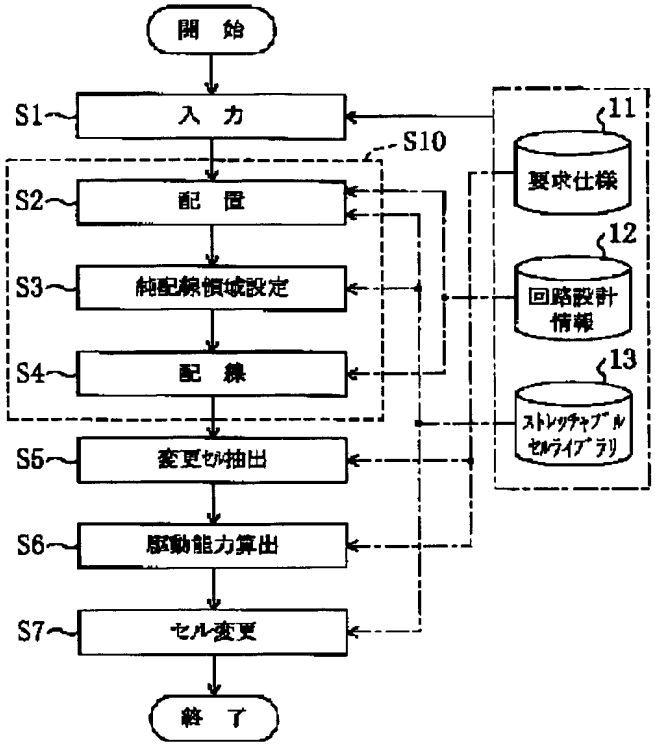
TITLE : METHOD AND DEVICE FOR DESIGNING LSI LAYOUT, CELL LIBRARY AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



ABSTRACT : PROBLEM TO BE SOLVED: To provide a method for designing an LSI layout by which variations in wiring delay time due to change of cell are minimized, and desired specifications can be satisfied with reliability in a short time.

SOLUTION: Cells are disposed in parallel according to circuit design information 12 (wiring operation S2). At the same time, wiring between the cells is performed (wiring operation S4) to design a block layout comprising multiple cell rows. Cells which do not satisfy desired specifications 11 are extracted from the block layout as cells to be changed (changing cells extracting operation S5). Driving ability which is necessary for satisfying the desired specifications 11 is calculated (driving ability calculating operation S6). Then, the cells to be changed are changed into cells with equivalent logic which are prepared in a stretchable cell library 13 and have a necessary driving ability and the same width and terminal position in the direction of the cell row (changing operation S7). In this case, a pure wiring area is set between cell rows (pure wiring area setting operation S3) to prevent design rule errors.